APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,630	01/25/2001	Hideo Miyake	1614.1116	5739

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EXAMINER
LI, AIMEE J

ART UNIT	PAPER NUMBER
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

	Application No.	Applicant(s)
Office Action Summary	09/768,630	MIYAKE ET AL.
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>28 December 2006 and 31 January 2007</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-5 and 18-20</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-5 and 18-20</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>25 January 2001</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>3/7/07</u>.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-5 and new claims 18-20 have been considered. Claims 6-17 have been

cancelled as per Applicant's request. New claims 18-20 have been added as per Applicant's

request.

Papers Submitted

2.   It is hereby acknowledged that the following papers have been received and placed of

record in the file: Amendment as filed 28 November 2006; RCE as filed 28 December 2006;

Amendment as filed 31 January 2007; and IDS as filed on 07 March 2007.

Continued Examination Under 37 CFR 1.114

3.   A request for continued examination under 37 CFR 1.114, including the fee set forth in

37 CFR 1.17(e), was filed in this application after final rejection. Since this application is

eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e)

has been timely paid, the finality of the previous Office action has been withdrawn pursuant to

37 CFR 1.114. Applicant's submission filed on 28 December 2006 has been entered.

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5.   Claims 1-5 and 18-20 are rejected under 35 U.S.C. 102(b) as being taught by Golliver et

al., U.S. Patent Number 5,928,356 (herein referred to as Golliver).

6.   Referring to claims 1, 3, 4, 5, 18, 19, and 20, taking claim 3 as exemplary, Golliver has

taught a computer which performs parallel processing of a plurality of programs in a time-

division fashion (Golliver Abstract "…the processor executes instructions from a particular task

for a period or time…"; column 2, lines 58-60 "Reference is also made to 'threads'…"; column

5, lines 7-10 "The context switch can be initiated in response to any of a wide variety of

conditions, such as the current time slice expiring…"; and column 8, lines 8-11 "…it should be

noted that 'context switching' as used herein refers to the switching of tasks…as well as the

switching of threads…"), comprising:

   a.   A memory (Golliver column 3, lines 59 to column 4, line 3 "…swapping of

           register contents between the register 110 and 115 and memory…");

   b.   An instruction fetch unit configured to fetch instructions from said memory

           (Golliver column 8, lines 38-44 "The instruction fetch and decode logic 815

           fetches instructions from memory…" and Figure 8, element 815);

   c.   Hardware resources divided into a plurality of areas, the hardware resources being

           used in common by a plurality of programs (Golliver column 3, lines 1-8 "…Each

           of the floating point registers 115 can be used by tasks or processes…"; column 4,

           lines 4-32 "…By logically separating the floating point registers 115 into two

           separate groups…"; and Figure 1, elements 115, Group 116 and Group 117);

   d.   An evacuation unit configured to record identification information identifying a

           first program (Golliver column 3, line 59 to column 4, line 3 "…Swapping of

           register contents refers to the saving of the current contents of the registers to

           memory…and the restoring of previously saved contents into the registers…" – In

regards to Golliver, when the data is saved and retrieved from memory, it is based on an identifier of some sort that lets the system know that the data being saved and restored belong to the correct threads.), and to evacuate information stored in a first area of said plurality of areas if the first area and a second area of said plurality of areas are necessary for execution of a second program and are being used for execution of the first program (Golliver column 6, line 36 to column 7, line 41 "...if the MDL bit is set, then the low group of floating point registers is saved...If the mdh bit is set, then the high group of floating point registers is saved..."; Figure 6; and Figure 7), said evacuation unit subsequently evacuating information stored in the second area when use of the second area becomes actually necessary for execution of the second program (Golliver column 6, line 36 to column 7, line 41 "...if the MDL bit is set, then the low group of floating point registers is saved...If the mdh bit is set, then the high group of floating point registers is saved..."; Figure 6; and Figure 7), said information being evacuated to a portion of said memory that corresponds to the first program (Golliver column 3, lines 59 to column 4, line 3 "...swapping of register contents between the register **110** and **115** and memory..."); and

e.   A restoration unit configured to restore, from the memory to the first area, a first part of information necessary for execution of the second program (Golliver column 3, line 59 to column 4, line 3 "...Swapping of register contents refers to...the restoring of previously saved contents into the registers..."), to mark the first area as a usable area while marking areas other than the first area as unusable

areas (Golliver column 4, line 59 to column 5, line 50 "...When an access to a

floating point register is detected, step **405**, the register control logic checks

whether the access is to the high group, step **410**, or to the low group, step

412..."; and Figure 4), to restore, from the memory to the second area, a second

part of the information necessary for execution of the second program (Golliver

column 3, line 59 to column 4, line 3 "...Swapping of register contents refers

to...the restoring of previously saved contents into the registers...") if execution

of the second program needs to use an area that is marked as an unusable area

(Golliver column 4, line 59 to column 5, line 50 "...When an access to a floating

point register is detected, step **405**, the register control logic checks whether the

access is to the high group, step **410**, or to the low group, step **412**..."; and Figure

4), and to restore the evacuated information to the first and second areas based on

the identification information when the second program comes to a halt or to an

end (Golliver column 3, line 59 to column 4, line 3 "...Swapping of register

contents refers to...the restoring of previously saved contents into the

registers...").

7.   Claims 1, 4, 5, 18, 19, and 20 have similar limitations to claim 3 and are rejected for

similar reasons. The only difference between claims 1 and 18 and claim 3 is that claims 1 and 18

does not have some limitations found in claim 3 and are, therefore, broader in scope. The only

difference between claims 4, 5, 19 and 20 is that claims 4, 5, 19, and 20 are method claims while

claim 3 is a computer claim. Also, claims 4, 19, and 20 are similar to claims 1 and 18 in that

they are broader in scope than claims 3 and 5.

8.   Referring to claim 2, Golliver has taught the computer as claimed in claim 1, further

comprising an interruption unit which brings about interruption processing if the first area is

necessary for execution of a second program and is being used for execution of the first program

(Golliver column 5, lines 4-17 "...The context switch can be initiated..." and Figure 3), wherein

said evacuation unit operates as part of the interruption processing to record the identification

information and to evacuate the information stored in the first area (Golliver column 6, line 36 to

column 7, line 41 "...if the MDL bit is set, then the low group of floating point registers is

saved...If the mdh bit is set, then the high group of floating point registers is saved..."; Figure 6;

and Figure 7).

Response to Arguments

9.   Applicant's arguments with respect to claims 1-5 and 18-20 have been considered but are

moot in view of the new ground(s) of rejection.

Conclusion

10.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

a.   Sharangpani et al., U.S. Patent Number 5,710,562; 5,729,724; and 7,740,093,

have taught sharing registers among threads and saving and restoring the registers

to and from dedicated memory in response to context switches.

b.   Bucher, U.S. Patent Number 5,421,014, has taught a multi-threaded system which

saves and restores contexts and uses thread Ids to identify threads.

c.   Wong, U.S. Patent Number 6,145,049, has taught storing contexts in main

memory and restoring therefrom an associated shadow register file.
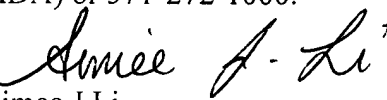
d.   Hinds et al., U.S. Patent Number 6,170,001has taught a shared register bank that are stored temporarily to memory on a context switch and subsequently retrieved.

e.   Jensen et al., U.S. Patent Number 6,587,937, has taught storing thread contexts in cache memory and restoring therefrom.

f.   Dave Marshall's Threads: Basic Theory and Libraries ©January 1999 has taught the basics of thread processing and identifying individual threads.

11.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

12.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

13.   Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aimee J Li

Art Unit 2183

29 March 2007